REMARKS/ARGUMENTS

By this paper, Applicant responds to the Office Action of May 20, 2005 and respectfully requests reconsideration of the application. A Petition for Extension of Time extends the shortened statutory period through September 20, 2005. Accordingly, this response is timely.

I. Real Party in Interest

The real party in interest is ATI International SRL of Barbados, the assignee of this application. ATI International is related to ATI Technologies, Inc. of Ontario, Canada.

II. Related Appeals and Interferences

Applicant is unaware of any related appeals or interferences.

III. Status of Claims

Claims 1-59 and 61-65 are now pending, a total of 64 claims. Claims 1, 2, 14, 22, 30 40 and 55 are independent. All rejections are traversed.

A complete copy of the claims is attached hereto as an Appendix.

IV. Status of Amendments

The amendments enclosed herewith may be entered as a matter of right.

V. Informal Summary of the Subject Matter

Generally, the claims relate to detecting reordered side-effects, or other changes to execution of instructions that may have a material effect on execution, and making appropriate corrections. To over-simplify the definition, "side effects" are the architecturally-visible effects on processor or memory state by which each instruction stores its results for use by following instructions. Side-effects may be reordered when a processor reorders instructions for execution in a pipeline, when a binary translator translates from one instruction set to another, when an optimizing compiler reorganizes code, etc.

Because the only issues relate to double patenting, and the examiner's errors are nearly all either failures to address essential legal elements or applications of incorrect legal tests, no detailed summary of the subject matter is necessary.

VI. Argument

As noted below, the Office Action of May 20, 2005 is too incomplete to raise any rejection of any claim. No rejections exist. Further, because the Office Action is silent on so many points, it is impossible to directly respond to whatever position the examiner might hold. Applicant will make a best attempt to guess at the examiner's position, but it should be understood that these are only guesses. If the examiner clearly and completely states positions in the future, they will be "new grounds of rejection" that prevent final rejection.

A. Issues Relating to the '379 Patent

1. Incomplete Analysis

First Error. The Office Action makes no *bona fide* effort to identify the differences between the instant claims and the '379 claims. Without even a minimal attempt to identify differences, the Office Action then omits any consideration of the obviousness of those differences. For example, here are the claim pairs set forth in the Office Action. The claims differ to at least the extent underlined. The Office Action is simply silent on almost every difference. The Office Action is too incomplete to raise any rejection.

Instant claim 2+3	'379 Patent Claims 4+78
2. A method, comprising the step of:	4. A method, comprising the steps of:
for memory references generated as part of executing a stream of instructions on a computer, evaluating whether an individual memory reference of an instruction references <u>a device having a valid memory address</u> but that cannot be guaranteed to be well-behaved, based at least in part on an annotation encoded in a segment descriptor.	
	<u>issuing a successful memory reference from a computer CPU to a bus;</u>
	<u>recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not-well-behaved memory.</u>
3. A method of claim 2, further comprising the step of:	7. The method of claim 4, further comprising the steps of:

if the reference cannot be guaranteed to be well-behaved, re-executing the instruction in an alternative execution mode.	evaluating whether an individual memory reference of an instruction references a device that cannot be guaranteed to be well-behaved, and if the reference cannot be guaranteed to be well-behaved, re-executing the instruction in an alternative execution mode.

Instant claim 14+17	**'379 Patent Claims 4+8**
14. A computer, comprising:	4. A method, comprising the steps of:
instruction execution circuitry designed to evaluate, based at least in part on an annotation encoded in a segment descriptor, whether an individual memory-reference instruction, or an individual memory reference of an instruction, references a device with a valid memory address that cannot be guaranteed to be well-behaved.	
	issuing a successful memory reference from a computer CPU to a bus;
	recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not-well-behaved memory.
17. The computer of claim 14, further comprising:	8. The method of claim 4, further comprising the steps of:
a translator programmed to translate at least a segment of a source program into an object program, wherein a sequence of side-effects in the object program differs from a reference sequence of side-effects in the source program; and	while translating at least a segment of a binary representation of a program from a first instruction set architecture to a second instruction set architecture, using the recording to distinguish memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory;
	while executing the translation into the second instruction set architecture, identifying loads that were believed at translation time to be directed to well-behaved memory but that at execution are found to be directed to non-well-behaved memory, and aborting the identified memory load;
	re-executing at least a portion of the translated segment of the program in the first instruction set.

circuitry and/or software designed to intervene during an execution of the object program on the computer to establish a program state equivalent to a state that would have occurred in the reference sequence, and to resume execution of the program from the established state in an execution mode that reflects the reference side-effect sequence.	

Instant claim 22	**'379 Patent Claims 4+8**
22. A method, comprising the steps of:	4. A method, comprising the steps of:
	issuing a successful memory reference from a computer CPU to a bus;
	recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not-well-behaved memory.
	8. The method of claim 4, further comprising the steps of:
while translating at least a segment of a binary representation of a program from a first instruction set architecture to a second representation in a second instruction set architecture, distinguishing individual memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory device(s);	while translating at least a segment of a binary representation of a program from a first instruction set architecture to a second instruction set architecture, using the recording to distinguish memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory;
while executing the second representation, identifying a load that was believed at translation time to be directed to well-behaved memory but that at execution time is found to be directed to non-well-behaved memory, based at least in part on an annotation encoded in a segment descriptor, and aborting the identified memory load; and	while executing the translation into the second instruction set architecture, identifying loads that were believed at translation time to be directed to well-behaved memory but that at execution are found to be directed to non-well-behaved memory, and aborting the identified memory load;
based at least in part on the identifying, re-executing at least a portion of the translated segment of the program in the first instruction set.	re-executing at least a portion of the translated segment of the program in the first instruction set.

Instant claim 30	**'379 Patent Claims 4+8**
30. An apparatus, comprising:	4. A method, comprising the steps of:
	issuing a successful memory reference from a computer CPU to a bus;

	recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not-well-behaved memory.
	8. The method of claim 4, further comprising the steps of:
a binary translator programmed to translate at least a segment of a binary representation of a program from a first instruction set architecture to a second representation in a second instruction set architecture, distinguishing individual memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory; and	while translating at least a segment of a binary representation of a program from a first instruction set architecture to a second instruction set architecture, using the recording to distinguish memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory;
instruction execution circuitry designed to execute the translated program in the second representation, and to identify, based at least in part on an annotation encoded in a segment descriptor, memory loads that were believed at translation time to be directed to well-behaved memory but that at execution time are found to be directed to non-well-behaved memory, and to abort the identified memory load.	while executing the translation into the second instruction set architecture, identifying loads that were believed at translation time to be directed to well-behaved memory but that at execution are found to be directed to non-well-behaved memory, and aborting the identified memory load;
	re-executing at least a portion of the translated segment of the program in the first instruction set.

Instant claim 40	**'379 Patent Claims 4+8**
40. A method, comprising the steps of:	4. A method, comprising the steps of:
	issuing a successful memory reference from a computer CPU to a bus;
	recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not-well-behaved memory.
	8. The method of claim 4, further comprising the steps of:
translating at least a segment of a source program into an object program, the source program instructing a reference execution with a reference sequence of side-effects, the object program instructing an execution in which the sequence of side-effects differs from the reference sequence;	while translating at least a segment of a binary representation of a program from a first instruction set architecture to a second instruction set architecture, using the recording to distinguish memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed

	to non-well-behaved memory;
during an execution of the object program on a computer, detecting a side-effect about to be committed to processor state in which the differing side-effect sequence may have a material effect on the execution of the program, and aborting the side-effect;	while executing the translation into the second instruction set architecture, identifying loads that were believed at translation time to be directed to well-behaved memory but that at execution are found to be directed to non-well-behaved memory, and aborting the identified memory load;
	re-executing at least a portion of the translated segment of the program in the first instruction set.
establishing a program state equivalent to a state that would have occurred in the reference execution; and	
resuming execution of the program from the established state in an execution mode that reflects the reference side-effect sequence.	

Instant claim 55	**'379 Patent Claims 4+8**
55. An apparatus, comprising:	4. A method, comprising the steps of:
	issuing a successful memory reference from a computer CPU to a bus;
	recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not-well-behaved memory.
	8. The method of claim 4, further comprising the steps of:
a binary translator programmed to translate at least segment of a program from a first representation in a first instruction set architecture to a second representation in a second instruction set architecture, a sequence of side-effects in the second representation differing from a sequence of side-effects in the translated segment of the first representation; and	while translating at least a segment of a binary representation of a program from a first instruction set architecture to a second instruction set architecture, using the recording to distinguish memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory;
instruction execution circuitry and/or software designed to	while executing the translation into the second instruction set architecture, identifying loads that were believed at translation time to be directed to well-behaved memory but that at execution are found to be directed to non-well-behaved memory, and aborting the identified memory load;

	re-executing at least a portion of the translated segment of the program in the first instruction set.
identify cases during execution of the second representation in which the difference in sequence of side-effects may have a material effect on the execution of the program, before committing the side-effect to processor state, and aborting the side-effect; and	
to establish a program state equivalent to a state that would have occurred in the execution of the first representation, and to resume execution of the program from the established state in an execution mode that reflects the side-effect sequence of the first representation.	

2. Improper and Incorrect Assertion of Inherency

Second error. The Office Action asserts that the limitation "based at least in part on an annotation encoded in a segment descriptor" is "inherent." The Office Action makes no attempt to comply with MPEP § 2112 (underline in MPEP):

> **IV. EXAMINER MUST PROVIDE RATIONALE OR EVIDENCE TENDING TO SHOW INHERENCY**
>
> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic....
>
> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." ... The Board reversed on the basis that the examiner did not provide objective evidence or cogent technical reasoning to support the conclusion of inherency.).

Here, the Office Action merely asserts that "the annotation" in the "segment descriptor" is inherent, without any "basis in fact or technical reasoning" to suggest that "an annotation encoded in a segment descriptor" is the only possible implementation of '379 claim 4+8. For example, a complete Office Action could show that the problem identified in the Office Action is necessary to all embodiments of '379 claim 4+8, and that claim 22 is the only possible solution

to the problem the Office Action identifies. But with no showing of "necessary," no rejection exists.

Third error. As MPEP § 2112 notes, any possible alternative is sufficient to defeat inherency. There are many such alternatives. First, binary translators and instruction execution circuitry have operated successfully for over a decade without any form of "annotation." Second, the annotation may be stored in a number of places other than the "segment descriptor," for example, in a TLB. The limitation is not inherent.

3. Failure to "Answer All Material Traversed"

Fifth error. MPEP § 707.07(f) reads as follows:

> **707.07(f) Answer All Material Traversed**
>
> ...
>
> Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it.

The "non inherency" of the "annotation" in "segment descriptors" was presented in a traverse in Applicant's paper of 2/28/05, at page 3 (section "Fourth," paragraphs (b) and (c)). For the examiner's convenience, that discussion is presented again here:

> **Fourth**, much of the analysis in the Office Action is inconsistent with facts already conceded by the Examiner. For example, claims 1-39 recite an event that occurs or action that is taken "based at least in part on an annotation encoded in a segment descriptor." The Office Action asserts that this is "inherent." The Office Action is incorrect in three respects:
>
> a) ...
>
> b) The Examiner appears to have already conceded that Cmelik '992 teaches an alternative to a "segment descriptor." Therefore this limitation does not "necessarily flow," and therefore is not inherent.
>
> c) The Examiner has already conceded that the "segment descriptor" of these claims provides a non-obvious distinction over Cmelik '992. The Office Action provides no basis to now assert the opposite, that "segment descriptors" are "obvious" over the claims of Yates '379.

The present Office Action does not answer this traverse. No rejection exists.

Applicant requests that any further assertion of "inherency" of the "annotations" in "segment descriptors" include a "basis in fact and/or technical reasoning to reasonably support the determination" in answer to the traverse in the February 2005 paper.

4. Incomplete Claims

Fifth Error. The May 2005 Office Action fails to recognize that many of the claims are dependent, and thus "shall be construed to incorporate by reference all the limitations of the claim to which it refers." 35 U.S.C. § 112 ¶ 4. For example, the comparison of "instant claim 22" to "'379 Patent Claim 8" set forth at pages 4-5 of the Office Action fails to recognize that claim 8 is dependent on claim 4, and ignores the limitations of claim 4 in the comparison. Without a correct comparison or identification of differences, or an explanation for why these limitations are ignored, the rest of the analysis in the Office Action is untrustworthy.

5. Request Under 37 C.F.R. § 1.104(d)(2)

Pursuant to 37 C.F.R. § 1.104(d)(2), if any rejection is raised in the future based on any assertion of "necessary" or similar reasoning not embodied in the patented claims themselves, Applicant requests a reference or an affidavit showing that the asserted matter was in fact known in the prior art.

B. Unidentified Issue Relating to the '181 Patent

Pages 5-9 of the Office Action raise an unidentified issue relating to the '181 patent.

1. The Office Action Does Not Identify Any Legal Basis

First Error. The Office Action does not even state that any claim is rejected, let alone identify the basis, or use the required MPEP form paragraphs. It is unclear whether any issue is being raised at all, let alone what the nature of the issue is.

The Office Action states that "instant claim 1 is anticipated by '181 patent claim 31." "Anticipation" invokes § 102, and rejection over prior art. However, the Office Action does not identify what paragraph of § 102 is involved, and thus it is difficult to respond. Further, this application claims priority back to August 30, 1999. The filing date of the '181 patent is later, November 3, 1999. Thus, at least for some claims, the '181 patent is not prior art. Further, the Office Action itself concedes that claim 22 has limitations that have no analogy in claim 31 of the '181 patent, and thus there cannot possibly be an anticipation.

The Office Action also suggests that there may be some form of double patenting issue, but does not identify whether the issue is "same invention" or "obviousness type" double patenting.

Applicant respectfully requests that in the future, all rejections be stated using an appropriate form paragraph from Chapter 700 of the MPEP, with showings of all *prima facie* elements specified by the MPEP.

Giving the Office Action the benefit of the doubt, Applicant will attempt to respond as if an obviousness-type double patenting issue was intended. This is not a concession that any rejection actually exists, only a good faith attempt to advance prosecution.

2. Erroneous Reliance on the Specification of the Prior Patent

Second error. Assuming that double patenting is the intended issue, then any double patenting rejection must rely solely on the claims. MPEP § 804(B)(1) ("the disclosure of the patent may not be used as prior art.") The Office Action relies on the specification of the '181 patent. See page 8 of the Office Action. This is examiner error.

3. Incomplete Identification Of Differences

Third error. The identification of differences between claim 1 of this application and claim 31 of the '181 patent is incorrect. Additional differences between the claims exist, as set forth below:

Instant claim 1	'181 Claim 29+31
1. (previously presented) A computer, comprising:	29. A method, comprising the steps of:
	translating a source program into an object program, the translated object program having a different execution behavior than the source program;
	when an interrupt occurs during execution of the object program, establishing a state of the program corresponding to a state that would have occurred during an execution of the source program, and from which execution can continue;
	executing the source program from the established state in a mode that executes or interprets the source program without re-translation into the language of the object program.
	31. The method of claim 29:

a binary translator programmed to translate at least a segment of a binary representation of a program from a first representation in a first instruction set architecture to a second representation in a second instruction set architecture, a sequence of side-effects in the second representation differing from a sequence of side-effects in the translated segment of the first representation, the second representation distinguishing individual memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory device(s);	while translating the source program from a first instruction set to the object program in a second instruction set, distinguishing individual memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory device(s);
instruction execution circuitry designed, while executing the second representation,	
to identify an individual memory-reference instruction, or an individual memory reference of an instruction, a side-effect arising from the memory reference having been reordered by the translator, the memory reference having been believed at translation time to be directed to well-behaved memory but that at execution time is found to reference a device with a valid memory address that cannot be guaranteed to be well-behaved, based at least in part on an annotation encoded in a segment descriptor, and	while executing the object program, identifying a load that was believed at translation time to be directed to well-behaved memory but that at execution is found to be directed to non-well-behaved memory, and aborting the identified memory load;
based in the distinguishing, to identify whether the difference in sequence of side-effects may have a material effect on the execution of the program; and	
circuitry and/or software designed to establish program state to a state equivalent to a state that would have occurred in the execution of the first representation, and to resume execution of the translated segment of the program in the first instruction set.	based at least in part on the identifying, re-executing at least a portion of the source program.

Without a *bona fide* attempt to identify the differences, the Office Action omits many showings of obviousness of the differences. Until an Office Action explains why every difference is obvious, and why the combination of all differences is obvious, no rejection exists.

4. Failure To Make Any Showing Of Obviousness Of A Differing "Sequence Of Side Effects"

Fourth error. The Office Action concedes that "a sequence of side-effects in the second representation differing from a sequence of side-effects in the translated segment of the first representation" is a difference between claim 1 of this application and claim 31 of the '181 patent. Page 7, lines 5-7. Yet the Office Action is silent on any showing that this difference is obvious. Without that showing, no rejection exists.

5. Incomplete And Incorrect Assertions Of "Inherency"

Fifth error. The Office Action asserts that "without the identification of side effects individual memory loads that are believed to be directed to well-behaved memory could not be distinguished from memory loads that are believed to be directed to non-well-behaved memory device." The Office Action cites no evidence that this problem was recognized before the effective filing date of this application, let alone that the solution recited in the claim was known to be an obvious solution to that problem. Anything unknown before the filing date cannot be obvious. Without some showing that it was known, no rejection exists. Pursuant to 37 C.F.R. § 1.104(d)(2), if any future rejection is based on any similar reason, Applicant requests a reference or an affidavit showing that the subject matter was known before the application's filing date.

Sixth error. An "annotation encoded in a segment descriptor" has not been shown to be inherent, is not inherent, and is not an obvious variant, for reasons analogous to those discussed with respect to the '379 patent, see sections "Second error," "Third error," and "Fourth error," in sections VI.A.2 and VI.A.3, at page 7, above.

VII. Dependent claims

The Office Action does not mention any defect in any of claims 4-13, 15, 16, 18-21, 23-29, 31-39, 41-54, 56-59 or 61-65, let alone make any showing that any of these claims correspond to any claim of either the '379 or '181 patent. Applicant requests either a clear indication in the next Office Action that these claims are allowable, or an element-by-element showing of any rejection.

VIII. Conclusion

Applicant notes that the examination of this application, at least for double patenting, has been extraordinarily sloppy. This is a waste of time for the examiner, and a waste of money for Applicant. Applicant respectfully requests a careful examination of the claims, in light of all differences indicated above.

In view of these remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. In the event that any extension of time is required, Applicant petitions for that extension of time required to make this response timely. Kindly charge any additional fee, or credit any surplus, to Deposit Account No. 23-2405, Order No. 114596-20-4009.

Respectfully submitted,

WILLKIE FARR & GALLAGHER LLP

Dated: September 20, 2005

By: _____

David E. Boundy
Registration No. 36,461

WILLKIE FARR & GALLAGHER LLP
787 Seventh Ave.
New York, New York 10019
(212) 728-8757
(212) 728-9757 Fax